

What is Claimed Is:

1. A semiconductor device comprising:
 - a layer of semiconductor material;
 - a plurality of regions of first and second opposite conductivity-types disposed in the layer of semi-conductor material;
 - one region of the plurality comprising an anode-emitter;
 - another region of the plurality of regions comprising a cathode-emitter;
 - the cathode-emitter of conductivity type opposite to that of the anode-emitter;
 - at least two regions of the plurality of regions disposed between the anode-emitter and the cathode-emitter;
 - the anode-emitter defining a junction where it meets one of the at least two regions;
 - a first electrode disposed over at least one of the regions between the anode and the cathode emitters; and
 - epitaxial material on the cathode and/or anode-emitter regions of the layer of semiconductor material;
 - the epitaxial material offset laterally from and clear of the junction of the anode and/or cathode emitter region(s) at the surface of the layer of semiconductor material.
2. The device of claim 1, further comprising silicide on at least a portion of the epitaxial material.
3. The device of claim 2, the first electrode comprising polysilicon and silicide on at least a portion of the polysilicon as a gate electrode.
4. The device of claim 2, in which

the epitaxial material comprises a peripheral edge where it meets the surface of the layer of semiconductor material; and

the layer of semiconductor material comprises a region between the peripheral edge of the epitaxial material and the first electrode that is free of silicide.

5. The device of claim 4,

the anode-emitter, the cathode-emitter, and the at least two different regions of the alternating regions therebetween defining a thyristor;

the two different regions between the anode and the cathode-emitters to establish first and second base regions respectively of the thyristor; and

the first electrode disposed over a substantial width of the second base region and over a portion of the cathode-emitter neighboring the second base;

the surface region free of silicide between the peripheral edge of the epitaxial material of the anode-emitter and a peripheral edge of the first electrode, extending laterally over a portion of the anode-emitter region, the full width of the first base region of the thyristor and a portion of the width of the second base region.

6. The device of claim 2, further comprising:

a conductor to propagate a reference voltage;

the conductor electrically coupled to the silicide of at least one of the anode and the cathode emitters.

7. The device of claim 6, in which:

the layer of semiconductor material further comprises source, drain and channel regions to define at least in part an access transistor;

one of the source and drain region of the access transistor in common with one of the cathode-emitter and the anode-emitter; and

the device further comprises:

a gate electrode over the channel region of the access transistor, the gate operable under voltage bias to apply an electric field to the channel region; and

epitaxial material on the other of the source and drain region;

silicide on the epitaxial material over the other of the source and the drain region; and

a bitline in electrical contact with the silicide of the other of the source and drain region.

8. The device of claim 7, further comprising:

first and second sidewall spacers against respective first and second opposite sidewalls of the first electrode;

the first sidewall spacer over the cathode-emitter and comprising a first lateral width that extends outward from the electrode; and

the second sidewall spacer comprising a lateral width that extends outward from the electrode by a distance substantially greater than the first lateral width.

9. The device of claim 8, further comprising:

epitaxial material on the shared emitter-source and drain region;

the epitaxial material on the emitter comprising a peripheral edge that is laterally offset from the first electrode by a magnitude related to the first lateral width of the first sidewall spacer; and

the epitaxial material of the anode-emitter laterally offset from the first electrode by a magnitude at least as great as the lateral width of the second sidewall spacer.

10. A memory device comprising:

a thyristor formed in a layer of semiconductor material, the thyristor comprising:

an anode-emitter;

a cathode-emitter; and

first and second base regions of different polarities between the anode-emitter and the cathode-emitter ;

a first electrode over at least a portion of and capacitively coupled to the first base region;

the second base region formed in a position of the layer of semiconductor material that is offset laterally and outwardly from an edge of the first electrode; and

a raised provision of semiconductor material on the layer of semiconductor material as a raised portion of at least one of the anode-emitter and cathode-emitter ;

the raised portion of the anode-emitter comprising sidewalls that define at least in part an outline at the surface of the layer of semiconductor material and spaced laterally from the second base region.

11. The device of claim 10, further comprising:

an access transistor to access the thyristor;

the access transistor comprising source, drain and body regions within the layer of semiconductor material, the body region in contiguous relationship between the source and drain regions; and

raised source and drain provisions on the layer of semiconductor material and over the respective source and drain regions.

12. The device of claim 11, one of the source and drain regions of the access transistor in common with one of the cathode-emitter and anode-emitter of the thyristor within the layer of semiconductor material.

13. The device of claim 11, in which the raised provisions for the anode-emitter, source and drain regions comprise epitaxial material.

14. The device of claim 13, the layer of semiconductor material comprising a layer of silicon over an insulator.

15. The device of claim 14, in which the thickness of the layer of silicon over the insulator is less than 50 nm.
16. The device of claim 11, further comprising silicide on at least one of the raised provisions of the anode-emitter, the source and the drain regions.
17. The device of claim 16, in which each of the thyristor electrode and a gate electrode of the access transistor comprise:

polysilicon in insulated relationship over the layer of semiconductor material; and

silicide on at least a portion of the polysilicon.
18. The device of claim 10, further comprising silicide-blocking material over the layer of semiconductor material and between the raised provision and the first electrode.
19. A method of semiconductor processing to form a thyristor memory device, comprising:

forming a wordline over a layer of silicon, the silicon of a first-type conductivity;

forming first dielectric over the wordline and the layer of silicon;

patterning the first dielectric to define a mask comprising a first part over at least a portion of the wordline, a second part contiguous with the first part and conformal to a sidewall of the wordline, and a third part contiguous with the second part as a shoulder that extends outwardly from the wordline and across a portion of the layer of silicon;

implanting dopant of second-type conductivity in the layer of silicon using an angled implant relative to the surface of the silicon and in self-alignment with the mask; and

after the implanting of the second-type conductivity dopant, implanting dopant of first-type conductivity in the layer of silicon using a substantially orthogonal implant angle and self-aligned with the salicide mask.
20. The method of claim 19, further comprising, after the first and second-type conductivity implants, siliciding exposed regions of silicon as defined by the salicide mask.

21. The method of claim 20, further comprising:

defining a cathode/anode-emitter region in the layer of silicon by implanting dopant of the second-type conductivity into regions of the layer of silicon that neighbor the wordline and at a side thereof opposite to the extended shoulder of the mask;

the implanting to define the cathode/anode-emitter region comprising:

using a mask defined at least in part by the wordline; and

accelerating the second-type dopant with a substantially orthogonal angle of incidence toward the layer of silicon.

22. The method of claim 21, in which the implanting of the second-type conductivity dopant comprises:

controlling at least one parameter of the group consisting of the acute angle of incidence, the implant energy, a lateral width of the shoulder and the implant species of the implanting to form a lateral extent for the second-type conductivity dopant as a first base region of the thyristor beneath the shoulder of the salicide mask; and

defining in part a boundary to a second base of the thyristor, the second base region comprising material of the layer of silicon of the first-type conductivity disposed between the first base region and the cathode/anode-emitter .

23. The method of claim 22, further comprising forming an access transistor in series with and coupled to the thyristor's cathode/anode-emitter region.

24. The method of claim 22, in which the patterning of the conformal layer of dielectric comprises forming the width of the shoulder of the mask with a lateral extend that is greater than its conformal thickness.

25. The method of claim 24, in which the patterning of the dielectric comprises:

forming a conformal layer of first dielectric over the wordline and layer of silicon;

forming a conformal layer of second dielectric over the layer of nitride, the second dielectric selectively etchable relative to the first dielectric; anisotropically etching the second dielectric until exposing portions of the first dielectric while using the first dielectric as an etch-stop, the anisotropically etching to form a spacer of the second dielectric against a portion of the first dielectric and along a sidewall of the wordline; and

using the spacer and the portion of the first dielectric together during the angled implant.

26. The method of claim 25, in which the first and second dielectric comprise nitride and oxide respectively.
27. The method of claim 26, further comprising anisotropically etching the layer of nitride while using the oxide spacer as the mask and defining the lateral extent for the shoulder of the salicide mask.
28. The method of claim 26, further comprising performing the implant of the first-type conductivity dopant while using the orthogonal angle of incidence and while using the oxide spacer and the nitride layer together as a mask to define an anode/cathode-emitter region for the thyristor.
29. The method of claim 20, in which the wordline is formed with polysilicon, and the siliciding comprises siliciding exposed regions of the polysilicon, the exposed regions defined at least in part by walls of the mask.
30. The method of claim 20, further comprising:
before the siliciding and after the implanting of second-type conductivity dopant, growing epitaxial silicon over exposed regions of the layer of silicon.
31. The method of claim 30, in which the siliciding comprises diffusing metal into a surface region of the epitaxial silicon to form a silicide.
32. The method of claim 31, in which:
the implanting of the first-type conductivity dopant forms an anode-emitter region of the

thyristor;

the growing of the epitaxial silicon forms epitaxial silicon over the anode-emitter region; and

the silicidation forms silicide on the epitaxial silicon over the anode-emitter region;

the method further comprising forming a contact on the silicide over the anode-emitter region, the contact for receiving a reference voltage.

33. The method of claim 32, further comprising:

implanting second-type conductivity dopant into a region of the layer of silicon aligned with a side of the wordline distal the anode-emitter and forming a cathode-emitter of the thyristor; and

forming an access transistor in series with the thyristor and coupled to the cathode-emitter.

34. The method of claim 33, in which the forming the access transistor comprises:

forming one of a drain and source for the access transistor in common with the thyristor's cathode-emitter; and

forming a bitline in electrical communication with the other one of the drain and the source of the access transistor.

35. A method of semiconductor processing comprising:

forming cathode/anode-emitter, first base, second base and anode/cathode-emitter regions to define a thyristor in a layer of silicon over an insulator;

forming a wordline over at least a portion of the first base region;

forming a salicide mask against a sidewall of the wordline and over a width of the region for the second base at the surface of the layer of silicon;

the second base region and the anode-emitter regions each formed with an alignment related at least in part to the salicide mask; and

implanting carrier lifetime adjustment species into one of the emitter base junction regions aligned at least in part to the salicide mask.

36. The method of claim 35, in which forming the salicide mask comprises covering the surface of the layer of silicon to overlap the width of the base region.
37. The method of claim 35, further comprising forming epitaxial silicon over exposed regions of the layer of silicon, the exposed regions to include the anode/cathode-emitter region and defined in part by the salicide mask.
38. The method of claim 37, further comprising forming silicide over exposed silicon defined in part by the salicide mask.
39. The method of claim 38, in which the implanting of the carrier lifetime adjustment species is performed after forming the epitaxial silicon and before forming the silicide.
40. The method of claim 39, in which the implanting the carrier lifetime adjustment species comprises using an implant energy to implant an upper region of the layer of silicon of a depth less than its thickness.
41. The method of claim 40, in which the implanting the carrier lifetime adjustment species comprises overlapping the interface between the anode/cathode-emitter and the second base with at least some of the implant species.
42. The method of claim 41, in which the implanting the carrier lifetime adjustment species defines a region thereof that remains clear of the junction between the first base and the second base.
43. The method of claim 41, further comprising using at least one particle ion species of the group consisting of column IV, column VIII or refractory metal elements to influence a leakage characteristic of the interface.
44. The method of claim 41, in which the implanting the carrier lifetime adjustment species further comprising accelerating the species toward the layer of silicon with an acute angel of incidence.
45. A method of forming a thyristor memory device, comprising:

forming first and second wordlines over a layer of silicon;

forming source and drain regions for an access transistor in the layer of silicon about respective sides of the first wordline, the source and the drain regions formed to define a channel region therebetween and beneath the first wordline;

forming first and second spacers against opposite sidewalls of the second wordline; the forming the first and the second spacers comprising:

forming the first spacer against an anode/cathode-emitter sidewall of the second wordline,

forming the second spacer against a cathode/anode-emitter sidewall of the second wordline opposite the anode/cathode-emitter sidewall, and

forming the first spacer with a width that extends over the layer of silicon and outward from the second wordline by a magnitude greater than that for the second spacer;

forming a cathode/anode-emitter region for a thyristor in the layer of silicon aligned to the second spacer against the cathode/anode-emitter sidewall of the second wordline, and in common with the one of the source and drain regions for the access transistor;

forming a first base region for the thyristor in the layer of silicon beneath the first spacer and aligned relative thereto; and

forming an anode/cathode-emitter region for the thyristor in the layer of silicon laterally outward from and aligned relative to the first spacer.

46. The method of 45, in which the forming the first base region and the forming the cathode/anode-emitter region comprises defining a second base region for the thyristor therebetween and with a width at the surface of the layer of silicon that is substantially beneath the second wordline.
47. The method of claim 45, further comprising forming the layer of silicon of thickness less than 50 nm over an insulator.
48. The method of claim 45, in which the forming the first base region comprises:

implanting second-type conductivity dopant into the layer of silicon, the second-type conductivity opposite a first-type conductivity of the layer of silicon;

using the first spacer as part of a mask during the implant; and

penetrating regions of the layer of silicon beneath the first spacer with some of the second-type conductivity dopant.

49. The method of claim 48, further comprising using an angled implant for the dopant of the second-type conductivity.

50. The method of claim 49, in which the implanting with the second-type conductivity dopant comprises using an implant energy to penetrate a full depth of exposed regions of the layer of layer of silicon.

51. The method of claim 50, in which the formation of the anode/cathode-emitter region comprises:

implanting an exposed region of the layer of silicon with first-type conductivity dopant;

defining the exposed region at least in part by the first spacer; and

using a substantially orthogonal angled implant for the implanting of the first-type conductivity dopant.

52. The method of claim 51, in which the implanting with the first-type conductivity dopant comprises:

using an implant energy to penetrate a partial depth of the layer of silicon; and

defining a sublayer of the second-type conductivity between the anode/cathode-emitter and the insulator.

53. The method of claim 51, further comprising:

forming an isolation trench between regions of the layer of silicon;

the formation of the anode/cathode-emitter in the layer of silicon to establish a sidewall thereof

facing the trench; and

forming insulating material in at least a portion of the isolation trench;

a sidewall of the trench defined at least in part by the anode/cathode-emitter.

54. The method of claim 53, in which the forming the isolation trench comprises:

forming a sidewall in the layer of silicon;

exposing an upper layer portion in the layer of silicon for the anode/cathode-emitter; and

exposing a lower layer portion in the layer of silicon of the second-type conductivity beneath the anode/cathode-emitter.

55. The method of claim 53, further comprising:

diffusing metal into exposed surface regions of the layer of silicon to form a silicide; and

defining the exposed surface regions at least in part by the first spacer and the partial fill of insulating material.

56. The method of claim 55, further comprising:

forming epitaxial silicon on the anode-emitter region of the layer of silicon and between a peripheral edge of the first spacer and the isolation trench; and

performing the metal diffusion to form the silicide after the formation of the epitaxial silicon and to silicide a surface region of the epitaxial silicon.

57. The method of claim 56, in which the metal diffusion comprises:

siliciding exposed sidewalls of the layer of silicon facing the isolation trench; and

diffusing a portion of the metal to a region of the sublayer proximate the isolation trench.